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ECE 2330
Prof. Crockett
LA10_memory_mapped_IO
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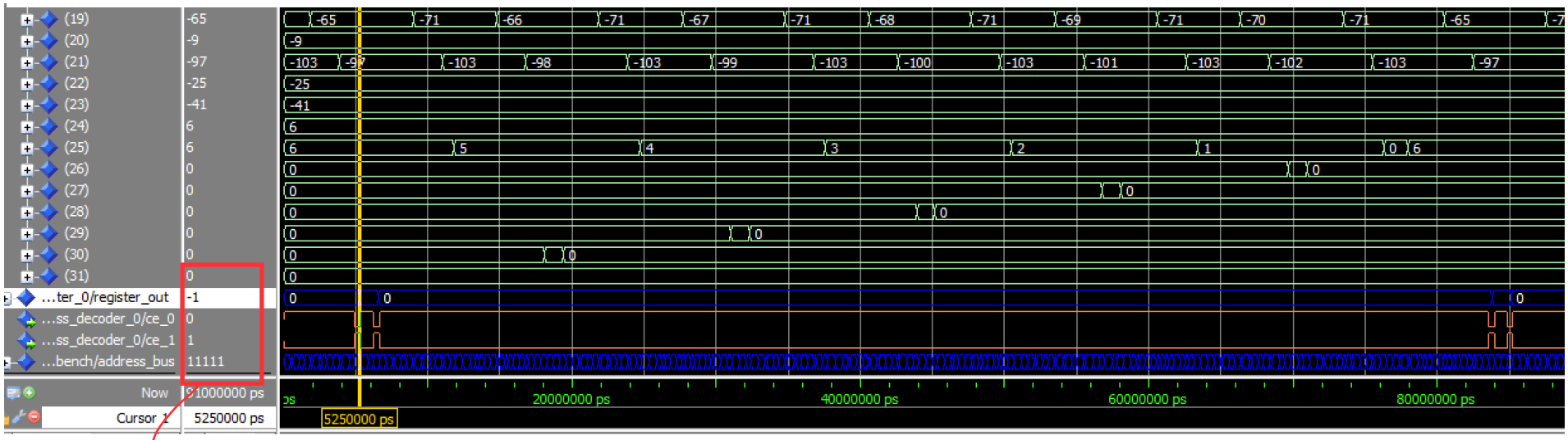
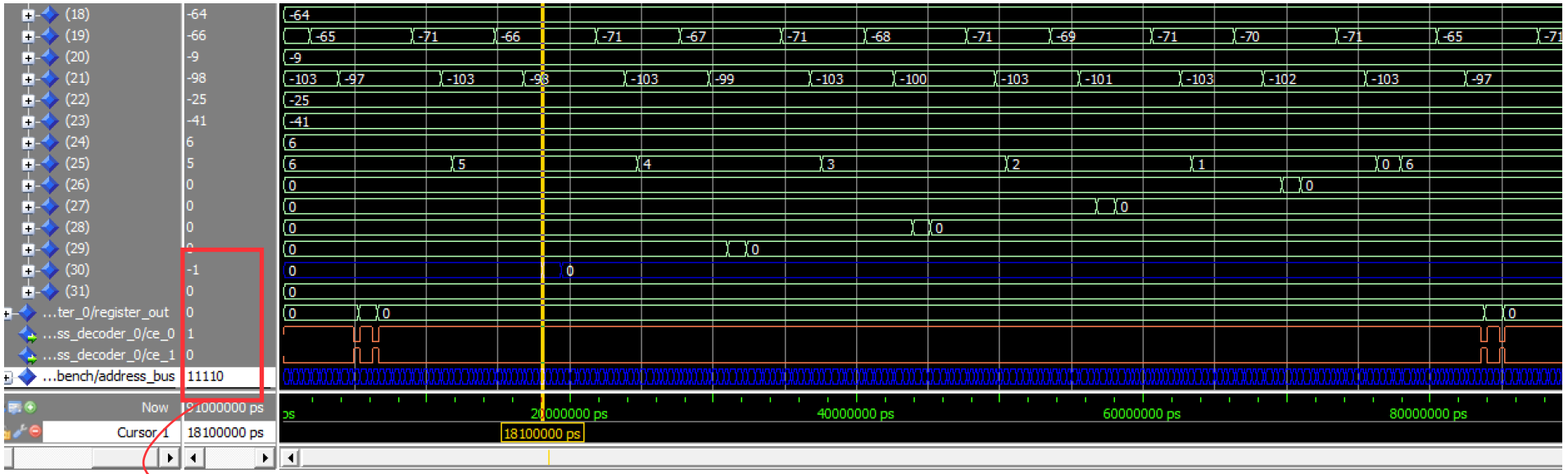
The following waveforms, indicated signals, and bulletpoints verify that my design meets the specifications of the assignment.



These signal values indicate that:
* my simple_cpu is accessing the port_register when ce_1 = 1
* my address_decoder output is {ce_0 = 0, ce_1 = 1} only when address_bus = 11111 (31)



These signal values indicate that:
* my simple_cpu is accessing the specified memory address (in this case 0x1E) when ce_0 = 1
* my address_decoder output is {ce_0 = 1, ce_1 = 0} when address_bus != 11111 (31)